

## Description

The G10N10A uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

## General Features

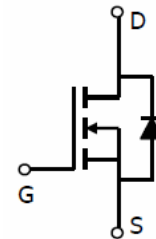
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$V_{DSS}$	$R_{DS(ON)}$ @10V (typ)	$R_{DS(ON)}$ @ 4.5V (typ)	$I_D$
100V	16m $\Omega$	18m $\Omega$	10A

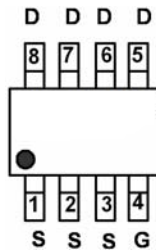
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current

## Application

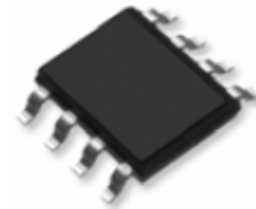
- DC/DC Primary Side Switch
- Telecom/Server
- Synchronous Rectification



Schematic diagram



Marking and pin assignment



SOP-8

## Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	10	A
Drain Current-Continuous( $T_C=100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	7	A
Pulsed Drain Current	$I_{DM}$	70	A
Maximum Power Dissipation	$P_D$	3.1	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

## Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	40	$^\circ\text{C/W}$
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## Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

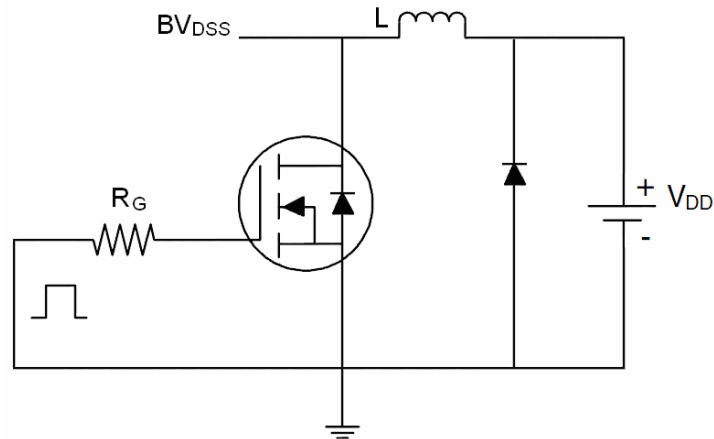
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.3	1.6	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=10A$	-	16	20	m $\Omega$
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=10A$	-	18	22	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=10A$	-	26	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	$C_{ISS}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2600	-	PF
Output Capacitance	$C_{OSS}$		-	590	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	291	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=10A, R_L=5\Omega,$ $R_G=1\Omega, V_{GS}=10V$	-	13	-	nS
Turn-on Rise Time	$t_r$		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	25	-	nS
Turn-Off Fall Time	$t_f$		-	10	-	nS
Total Gate Charge	$Q_g$	$I_D=10A, V_{DD}=50V, V_{GS}=10V$	-	90	-	nC
Gate-Source Charge	$Q_{gs}$		-	16	-	nC
Gate-Drain Charge	$Q_{gd}$		-	24	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-	0.85	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	10	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = 10A$	-	33		nS
Reverse Recovery Charge	$Q_{rr}$	$di/dt = 100A/\mu s$ (Note 3)	-	54		nC

### Notes:

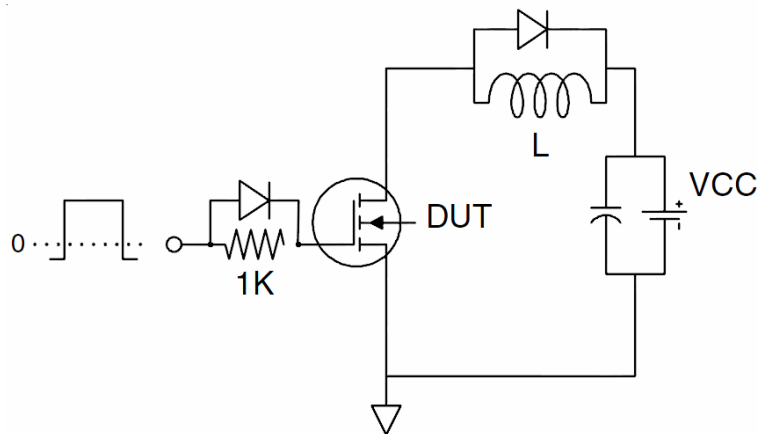
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

## Test Circuit

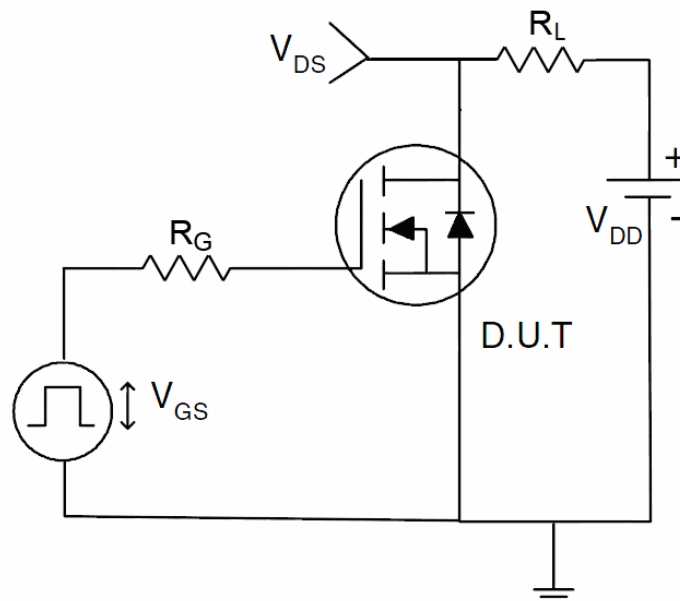
### 1) $E_{AS}$ test Circuit



### 2) Gate charge test Circuit



### 3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

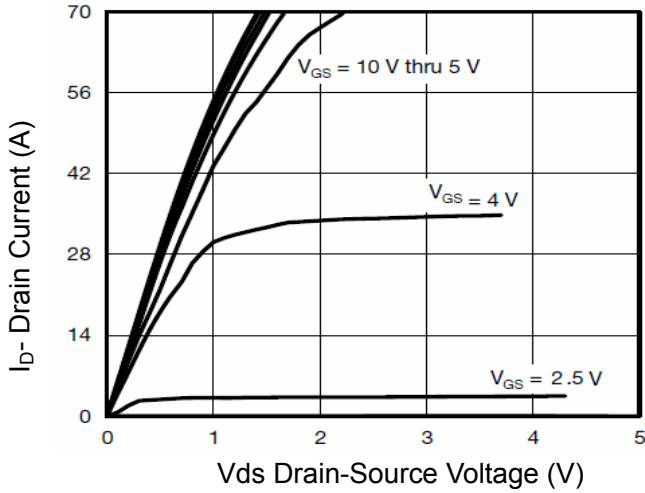


Figure 1 Output Characteristics

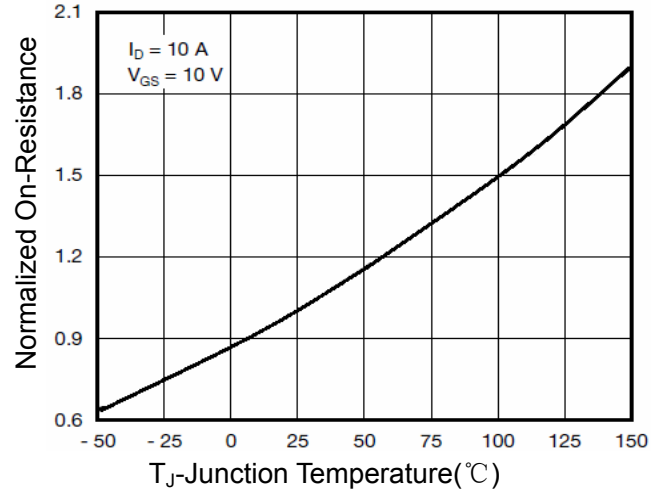


Figure 4  $R_{dson}$ -Junction Temperature

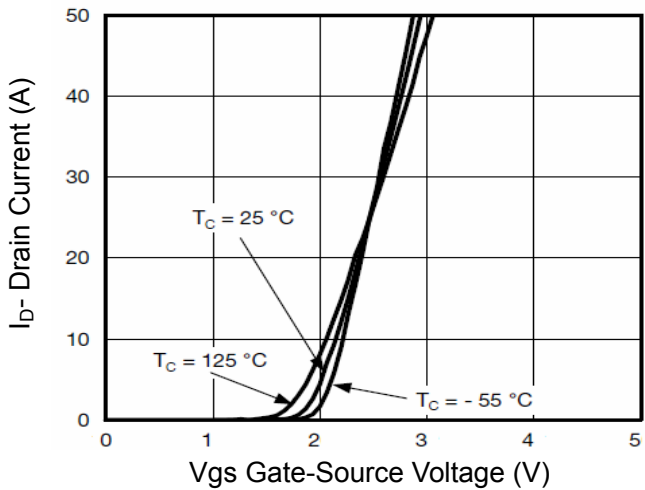


Figure 2 Transfer Characteristics

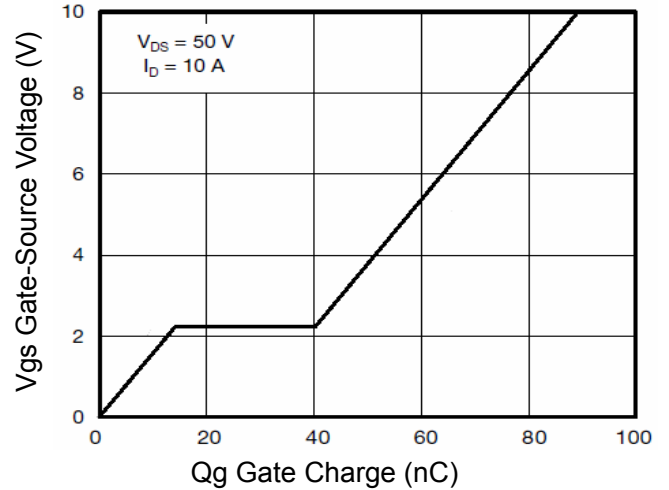


Figure 5 Gate Charge

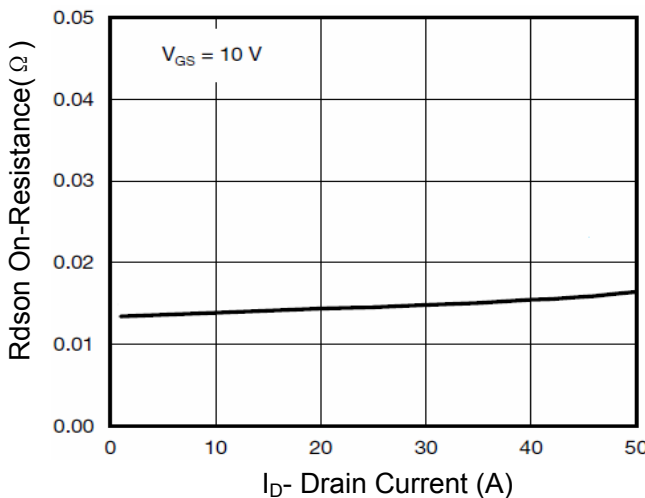


Figure 3  $R_{dson}$ - Drain Current

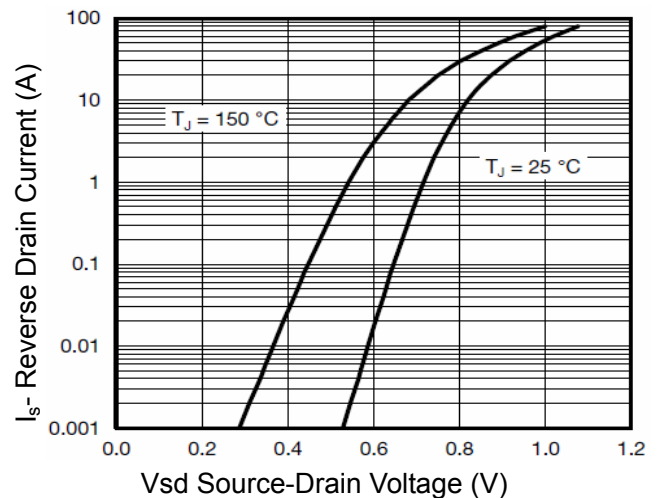


Figure 6 Source- Drain Diode Forward

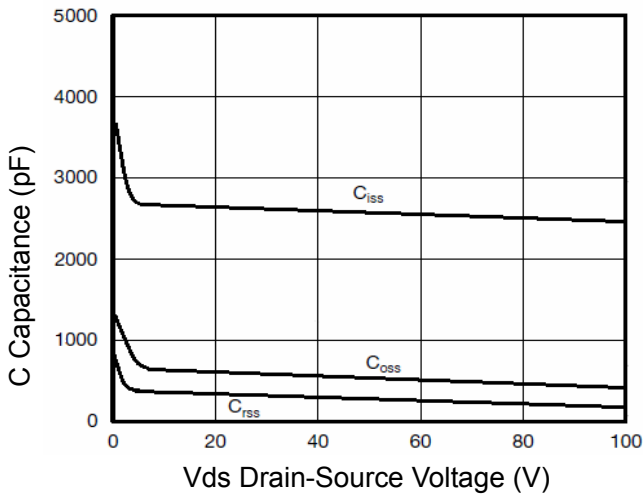


Figure 7 Capacitance vs Vds

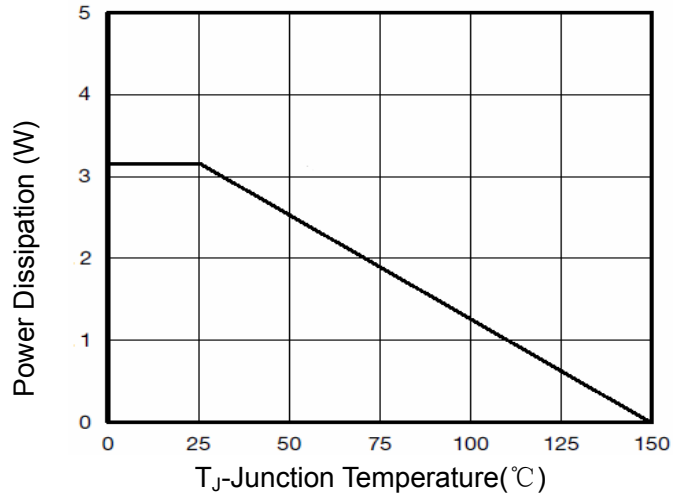


Figure 9 Power De-rating

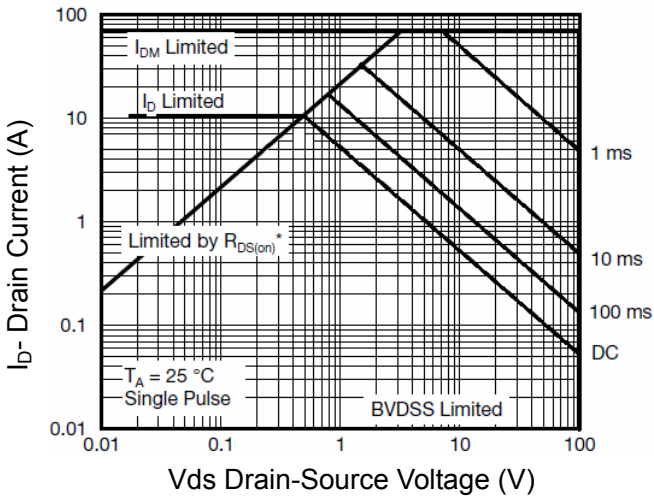


Figure 8 Safe Operation Area

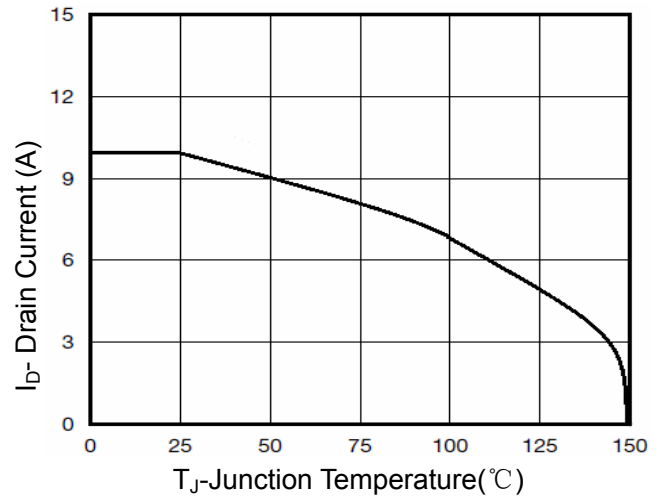


Figure 10 Current De-rating

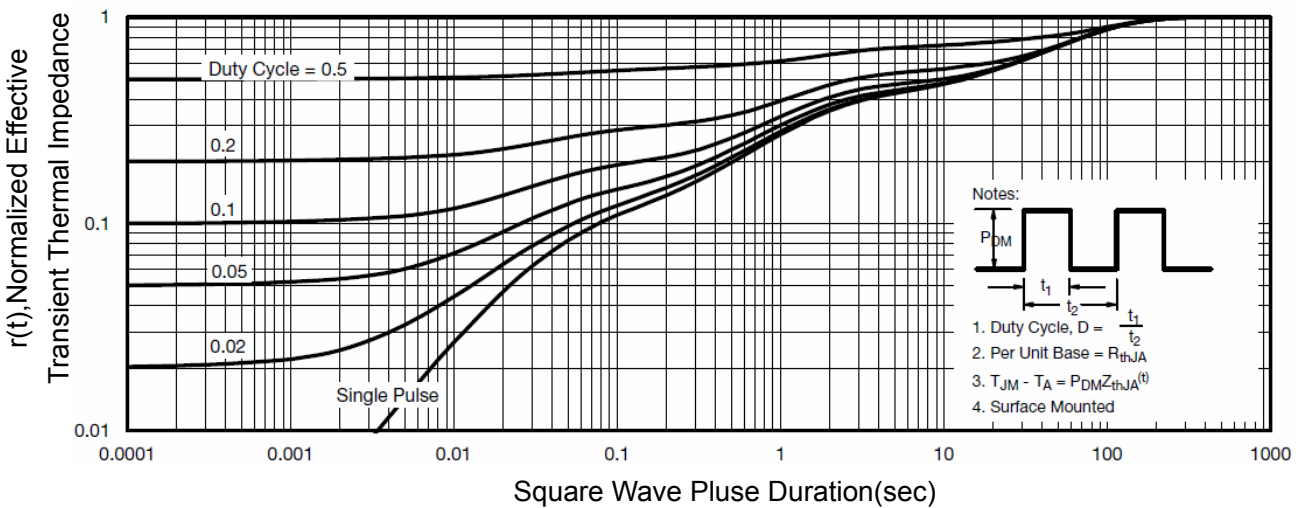


Figure 11 Normalized Maximum Transient Thermal Impedance